AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 8, lines 9-26 with the following amended paragraph:

Each sub-array comprises 1024 rows and 1024 columns in eight layers. This structure provides a main 1 MB storage element. Accordingly, the memory array 150 can store 64 MB of main data and 8 MB of syndrome bits for that data. Each sub-array also comprises eight additional rows for redundancy (in each layer). Redundancy/self-repair operations are described in "Memory Device and Method for Redundancy/Self-Repair," U.S. patent application serial no. 10/024,646, filed December 14, 2001 ~~(attorney docket no. 10519/31; filed on the same day as the present application)~~, which is assigned to the assignee of the present application and is hereby incorporated by reference. Further, each sub-array also comprises eight rows and four columns of test memory, half along each side of the sub-array, which contain sacrificial test bits. Alongside the 72 full sub-array elements, there are 16 smaller sub-arrays positioned in the columns along the two outer edges of the core array. The smaller sub-arrays are about ¼ the size of the full sub-arrays. Two sub-arrays on the same stripe are logically merged into a single element with 1024 rows and 512 columns. These smaller sub-arrays will be referred to herein as "spare arrays." The spare arrays are used to store sideband data, ECC bits for the sideband data, and data used for redundancy/self repair, all of which will be referred to herein as "spare data" (as compared to main data). As mentioned above, the memory array 150 in this preferred embodiment is byte addressable.

Please replace the paragraph at page 10, line 15 to page 11, line 5 with the following amended paragraph:

As discussed above, the spare array in Bay 9 is physically made up of two ¼-sized sub-arrays that logically act as a single array of 1024 rows and 512 columns (excluding redundancy and sacrificial test areas). To enable maximum separation between bits of an oct-byte in the spare array, bits are sprinkled within the page register 140. To simplify the interface between the page register 140 and the control logic, each page sub-register preferably is extended to hold a section of the spare array data as shown in Figure 8. The addition extends the sub-register by another bit (from eight to nine) for half of its height. As the page register 140 is made of nine sub-registers, the spare array data will be contained within the extended sections of these sub-registers as shown in Figure 9. In Figure 9, each block represents one byte of data (one bit wide and eight bits deep). SP0 and SP1 are the spare array data (16-bytes) and ECC0 and ECC1 are their respective ECC syndrome bits. XY is used to store redundancy/self-repair data, as described in "Memory Device and Method for Redundancy/Self-Repair," U.S. patent application serial no. 10/024,646, filed December 14, 2001 ~~(attorney docket no. 10519/31; filed on the same day as the present application)~~, which is assigned to the assignee of the present application and is hereby incorporated by reference. R is a reserved area, which can be used to store dynamic bit inversion information, as described in "Memory Device and Method for Dynamic Bit Inversion," U.S. patent application serial no. 10/023,466, filed December 14, 2001 ~~(attorney docket no. 10519/64; filed on the same day as the present application)~~, which is assigned to the assignee of the present application and is hereby incorporated by reference. XYM and RM are masked bit locations in XY and R space.